SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND ITS MANUFACTURING METHOD

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Publication date: 2002-01-25

Inventor(s): ODA KATSUYA; WASHIO KATSUYOSHI +

Applicant(s): HITACHI LTD +

Classification:

- international: ***H01L21/02; H01L21/205; H01L21/265; H01L21/331; H01L21/76; H01L21/762; H01L21/8222; H01L27/082; H01L27/12; H01L29/165; H01L29/73;* H01L21/02; H01L21/70; H01L27/082; H01L27/12; H01L29/02; H01L29/66;** (IPC1-7): H01L21/205; H01L21/265; H01L21/331; H01L21/76; H01L21/762; H01L21/8222; H01L27/082; H01L27/12; H01L29/165; H01L29/73

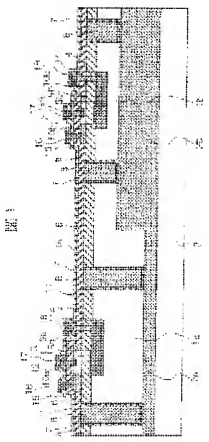
- European:

Application number: JP20000208244 20000705

Priority number(s): JP20000208244 20000705

Abstract of **JP 2002026137 (A)**

PROBLEM TO BE SOLVED: To provide a semiconductor integrated circuit device which has bipolar transistors with different cut-off frequencies and dielectric strengths, formed on the same semiconductor chip and its manufacturing method. SOLUTION: The bipolar transistors, having intrinsic base layers 9a and 9b with different thickness, are formed on the same semiconductor substrate 3. These base layers, having the thicknesses, can be formed at the same time by designing the thicknesses of insulating films formed between the semiconductor substrate 3 and low-density single-crystal silicon layers 1a and 1b. The performance of the circuit using the bipolar transistors can be made high. The need for using a diode to compensate for the dielectric strengths is eliminated, so that an increase in parasitic capacity due to addition of diode can be prevented, and the circuit can operate at a high speed.



SEMICONDUCTOR DEVICE FORMED OVER A MULTIPLE THICKNESS BURIED OXIDE LAYER, AND METHODS OF MAKING SAME

Publication number: WO03083934 (A1)

Publication date: 2003-10-09

Inventor(s): FUSELIER MARK B; WRISTERS DERICK J; WEI ANDY C +

Applicant(s): ADVANCED MICRO DEVICES INC [US] +

Classification:

- international: ***H01L21/02; H01L21/265; H01L21/336; H01L21/76; H01L21/762; H01L27/12; H01L29/786;*** **H01L21/02; H01L21/70; H01L27/12; H01L29/66;** (IPC1-7): H01L21/316; H01L21/335; H01L21/762

- European: H01L21/265A4; H01L21/336D3; H01L21/762D2; H01L29/786D

Application number: WO2002US40213 20021217

Priority number(s): US20020109096 20020328

Also published as:

US2004219761 (A1)

US6737332 (B1)

TW286821 (B)

JP2005522034 (T)

EP1490900 (A1)

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Cited documents:

EP0687002 (A2)

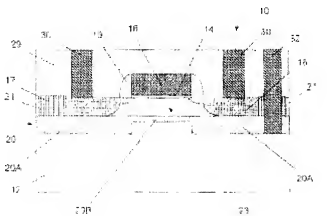
WO0048245 (A1)

US5950094 (A)

US6204546 (B1)

Abstract of **WO 03083934 (A1)**

The present invention is generally directed to a semiconductor device formed over a multiple thickness buried oxide layer 20, and various methods of making same. In one illustrative embodiment, the device comprises a bulk substrate 12, a multiple thickness buried oxide layer 20 formed above the bulk substrate 12, and an active layer 21 formed above the multiple thickness buried oxide layer 20, the semiconductor device being formed in the active layer 21 above the multiple thickness buried oxide layer 20. In some embodiments, the multiple thickness buried oxide layer 20 is comprised of a first section 20B positioned between two second sections 20A, the first section 20B having a thickness that is less than the thickness of the second sections 20A. In one illustrative embodiment, the method comprises performing a first oxygen ion implant process 42 on a silicon substrate 40, forming a masking layer 44 above the substrate 40, performing a second oxygen ion implant process 46 on the substrate 40 through the masking layer 44, and performing at least one heating process on the substrate 40 to form a multiple thickness buried oxide layer 20 in the substrate 40. In another illustrative embodiment, the method comprises performing a first oxygen ion implant process 46 on a silicon substrate 40, forming a masking layer 44 above the substrate 40, performing a second oxygen ion implant process 42 on the substrate through the masking layer 44, and performing at least one heating process on the substrate 40 to form a multiple thickness buried oxide layer 20 in the substrate 40. In yet another illustrative embodiment, the method comprises



forming a multiple thickness buried oxide layer 20
using a wafer bonding technique.

MOS-TYPE SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURE THEREOF

Publication number: JP7263575 (A)

Publication date: 1995-10-13

Inventor(s): IKEDA TADASHI +

Applicant(s): SONY CORP +

Classification:

- international: ***H01L21/02; H01L21/762; H01L21/8242; H01L27/08; H01L27/10; H01L27/108; H01L27/12; H01L29/78; H01L29/786;*** **H01L21/02; H01L21/70; H01L27/08; H01L27/10; H01L27/108; H01L27/12; H01L29/66;** (IPC1-7): H01L21/762; H01L21/8242; H01L27/08; H01L27/108; H01L27/12; H01L29/786

- European:

Application number: JP19940055485 19940325

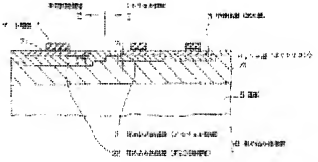
Priority number(s): JP19940055485 19940325

Also published as:

JP3254889 (B2)

Abstract of **JP 7263575 (A)**

PURPOSE:To provide a MOS type semiconductor device in which high integration and high speed can be realized at the same time and a method for manufacturing it in a MOS type semiconductor memory device having an SOI element.
CONSTITUTION:In a WAS type semiconductor memory device having the element of SOI structure, the film thickness of an insulating film 21 (oxide film in which a memory cell is buried, is thinner than the thickness 22 of a peripheral circuit.

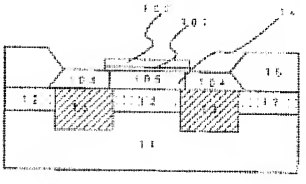


MOS SEMICONDUCTOR DEVICE AND FABRICATION THEREOF

Publication number: JP7078994 (A)
Publication date: 1995-03-20
Inventor(s): AOKI MASAAKI; OYU SHIZUNORI; MIYAMOTO MASABUMI +
Applicant(s): HITACHI LTD +
Classification:
- international: ***H01L21/265; H01L21/266; H01L29/78; H01L29/786;*** **H01L21/02; H01L29/66;** (IPC1-7): H01L21/265; H01L21/266; H01L29/786
- European:
Application number: JP19930221693 19930907
Priority number(s): JP19930221693 19930907

Abstract of **JP 7078994 (A)**

PURPOSE:To enhance the subthreshold characteristics and the current driving force by setting the thickness of an oxide buried under the channel part of an MOS transistor thinner than that under the diffusion layer. CONSTITUTION:Oxygen ions are implanted into a P-type Si substrate 11 which is then heat treated to form a buried oxide 12. The oxide is formed about 0.25mum thick in the depth direction with the center being about 0.19mum deep from the surface of Si. An SOI layer (Si crystal layer) 14 is then formed on the oxide 12 followed by formation of field oxide 15 by LOCOS. Subsequently, a gate oxide 101 (5-25nm thick) is formed on the SOI layer 14 followed by deposition of a polysilicon gate electrode layer 102. As ions are then implanted onto the SOI layer 14 with the gate electrode and the resist film thereon as masks thus forming the source 103, the drain part 104 and the channel part 105 of an nMOS transistor from an n+ diffusion layer. Oxygen ions are further implanted to form an oxide 13.



SOI SUBSTRATE AND MANUFACTURE THEREOF

Publication number: JP7263538 (A)

Publication date: 1995-10-13

Inventor(s): NAKASHIMA SADAO [JP]; IZUMI KATSUTOSHI [JP]; OHWADA NORIHIKO [JP]; KATAYAMA TATSUHIKO [JP] +

Applicant(s): KOMATSU DENSHI KINZOKU KK [JP]; NIPPON TELEGRAPH & TELEPHONE [JP]; NTT ELECTRONIC TECH [JP] +

Classification:

- international: ***H01L21/02; H01L21/265; H01L21/31; H01L21/76; H01L21/762; H01L21/86; H01L27/00; H01L27/12;*** **H01L21/02; H01L21/70; H01L27/00; H01L27/12;** (IPC1-7): H01L21/265; H01L21/76; H01L21/86; H01L27/00; H01L27/12

- European: H01L21/265A4; H01L21/762D2

Application number: JP19940076538 19940323

Priority number(s): JP19940076538 19940323

Also published as:

JP3036619 (B2)
EP0675534 (A2)
EP0675534 (A3)
EP0675534 (B1)
US5658809 (A)

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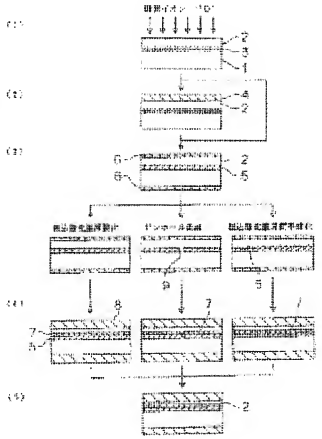
Abstract of **JP 7263538 (A)**

PURPOSE:To make a buried oxide film thick, reduce pin holes of the film, and increase the flatness of an interface between a silicon single crystalline layer on the surface and the buried oxide film, about the buried oxide film formed on the SIMOX substrate. CONSTITUTION:This is a method for manufacturing an SOI substrate wherein a buried oxide film is formed by implanting oxygen ions into a single crystalline silicon substrate and then conducting an annealing process that is a high-temperature heat treatment in an inactive gas atmosphere and after that a single crystalline silicon layer which is insulated from the substrate is formed on the surface. After conducting an annealing process wherein the thickness of the buried oxide film agrees with a logic value which is calculated by the implanted amount of oxygen ions, a substrate is oxidized in a high-temperature oxygen atmosphere.; In the high-temperature oxidation after the annealing process, oxygen of the density of 1% or above is supplied and the single crystalline silicon substrate 1 is oxidized at a temperature of 1150 deg.C or above and below a melting point of the substrate and then an oxide film is formed on a buried oxide film as an additional buried oxide film 7. By this method, the thickness of the buried oxide film is increased and thereby a pin hole 9 generated in the buried oxide film 5 is eliminated and an unevenness of an interface between the silicon single crystalline layer and the buried oxide film is eliminated and the interface is flattened.



MANUFACTURE OF SEMICONDUCTOR SUBSTRATE

Publication number: JP11040512 (A)

Publication date: 1999-02-12

Inventor(s): SAITO MINA; JAROSLOW JAVRONSKY; ANDO MASAHIKO; MIYAMURA KEIJI; KATAYAMA TATSUHIKO +

Applicant(s): KOMATSU DENSHI KINZOKU KK +

Classification:

- international: ***H01L21/02; H01L21/265; H01L27/12;*** **H01L21/02; H01L27/12;** (IPC1-7): H01L21/265; H01L27/12

- European:

Application number: JP19970211323 19970722

Priority number(s): JP19970211323 19970722

Also published as:

TW378353 (B)

Abstract of **JP 11040512 (A)**

PROBLEM TO BE SOLVED: To reduce a transition density present at a surface silicon layer of an SIMOX substrate, by performing annealing in a reducing atmosphere when an implanted oxygen atom reacts with a silicon to produce SiO2 . SOLUTION: An oxygen ion<16> O<+> is implanted to a single-crystal silicon substrate 10 by a specified depth using an ion implantation device. Thus, a high-concentration oxygen ion implantation layer 12 is formed. Here, the amount of implanted oxygen ion is less than 5× 10<17> /cm<2> . While an oxygen in the high- concentration ion implantation layer 12 implanted in a first process reacts with a silicon to produce SiO2 , thermal treatment is performed in a reducing atmosphere. After such ion implantation like this, when a low-temperature anneal process for thermal treatment in such reducing atmosphere as hydrogen at an early stage of thermal treatment formed by the SiO2 is ended, normal anneal process is performed. A crystal is stabilized with the anneal process, and the high-concentration oxygen ion implantation layer changes to an embedded oxide film 16.